AMENDMENTS TO THE CLAIMS

In accordance with 37 C.F.R. §1.121(c), please amend the claims as indicated in marked-up form below, where additions are underlined, deletions are struck through, and new claims are presented without markings.

Claim 1. (Withdrawn) A semiconductor component comprising:

a semiconductor substrate;

a first dielectric layer above the semiconductor substrate;

a first ohmic contact region above the semiconductor substrate;

a second ohmic contact region above the semiconductor substrate;

a gate electrode above the semiconductor substrate and between the first ohmic contact region and the second ohmic contact region;

a field plate above the first dielectric layer and between the gate electrode and the second ohmic contact region;

a second dielectric layer above the field plate, the first dielectric layer, the first ohmic contact region, and the second ohmic contact region; and

a third dielectric layer between the gate electrode and the field plate and not located above the gate electrode or the field plate.

Claim 2. (Withdrawn) The semiconductor component of claim 1 wherein:

the third dielectric layer isolates the gate electrode from the field plate.

Claim 3. (Withdrawn) The semiconductor component of claim 1 further comprising:

a semiconductor layer between the semiconductor substrate and the first dielectric layer.

Claim 4. (Withdrawn) The semiconductor component of claim 1 wherein:

the gate electrode comprises a T-gate electrode; and

the T-gate electrode comprises:

a titanium tungsten nitride layer; and

a gold layer above the titanium tungsten nitride layer.

Claim 5. (Withdrawn) The semiconductor component of claim 4 wherein:

a portion of the T-gate electrode overlies at least a portion of the field plate.

Claim 6. (Withdrawn) The semiconductor component of claim 1 wherein:

the gate electrode and the field plate are separated by a distance of between approximately 20 and 400 nanometers.

Claim 7. (Withdrawn) The semiconductor component of claim 1 wherein:

the field plate has a length of between approximately 300 and 2000 nanometers.

Claim 8. (Withdrawn) The semiconductor component of claim 1 wherein:

the field plate comprises titanium tungsten nitride.

Claim 9. (Withdrawn) The semiconductor component of claim 1 wherein:

the first dielectric layer has a thickness of between approximately 50 and 200 nanometers.

Claim 10. (Canceled)

Claim 11. (Currently Amended) ~~The method of claim 10 further comprising:~~ A method of manufacturing a semiconductor component, the method comprising:

providing a semiconductor substrate;

forming a first dielectric layer above the semiconductor substrate;

forming a field plate above the first dielectric layer;

self-aligning a gate electrode to the field plate; and

forming a first ohmic contact region and a second ohmic contact region above the semiconductor substrate,

wherein:

self-aligning the gate electrode to the field plate further comprises:

forming the gate electrode after forming the first ohmic contact region and the second ohmic contact region; and

forming the gate electrode to be between the first ohmic contact region and the second ohmic contact region.

Claim 12. (Currently Amended) The method of ~~claim 10~~ claim 11 further comprising:

forming a semiconductor layer above the semiconductor substrate before forming the first dielectric layer,

wherein:

forming the first dielectric layer comprises:

forming the first dielectric layer above the semiconductor layer.

Claim 13. (Currently Amended) ~~The method of claim 12 further comprising:~~ A method of manufacturing a semiconductor component, the method comprising:

providing a semiconductor substrate;

forming a first dielectric layer above the semiconductor substrate;

forming a field plate above the first dielectric layer;

self-aligning a gate electrode to the field plate;

forming a semiconductor layer above the semiconductor substrate before forming the first dielectric layer; and

forming a gate recess in the semiconductor ~~layer.~~ layer,

wherein:

forming the first dielectric layer comprises:

forming the first dielectric layer above the semiconductor layer.

Claim 14. (Currently Amended) The method of ~~claim 10~~ claim 11 wherein:

self aligning the gate electrode to the field plate further comprises:

forming a second dielectric layer above the field plate and the first dielectric layer;

forming a hole through the second dielectric layer to expose a portion of the field plate;

removing the portion of the field plate;

removing a portion of the first dielectric layer;

depositing a third dielectric layer over the second dielectric layer and in the hole;

etching the third dielectric layer to form a spacer inside the hole; and

forming the gate electrode in the hole.

Claim 15. (Currently Amended) ~~The method of claim 14 wherein:~~ A method of manufacturing a semiconductor component, the method comprising:

providing a semiconductor substrate;

forming a first dielectric layer above the semiconductor substrate;

forming a field plate above the first dielectric layer; and

self-aligning a gate electrode to the field plate,

wherein:

self aligning the gate electrode to the field plate further comprises:

forming a second dielectric layer above the field plate and the first dielectric layer;

forming a hole through the second dielectric layer to expose a portion of the field plate;

removing the portion of the field plate;

removing a portion of the first dielectric layer;

depositing a third dielectric layer over the second dielectric layer and in the hole;

etching the third dielectric layer to form a spacer inside the hole; and

forming the gate electrode in the hole; and

forming the second dielectric layer comprises:

forming the second dielectric layer to comprise:

a first tetra-ethyl-ortho-silicate layer;

an aluminum-nitride layer; and

a second tetra-ethyl-ortho-silicate layer.

Claim 16. (Original) The method of claim 15 wherein:

forming the second dielectric layer further comprises:

forming the aluminum-nitride layer between the first tetra-ethyl-ortho-silicate layer and the second tetra-ethyl-ortho-silicate layer.

Claim 17. (Currently Amended) The method of ~~claim 14~~ claim 15 wherein:

forming the gate electrode comprises:

forming a T-gate electrode having a titanium tungsten nitride layer.

Claim 18. (Original) The method of claim 17 wherein:

forming the T-gate electrode further comprises:

plating a gold layer above the titanium tungsten nitride layer.

Claim 19. (Currently Amended) ~~The method of claim 10 wherein:~~ A method of manufacturing a semiconductor component, the method comprising:

providing a semiconductor substrate;

forming a first dielectric layer above the semiconductor substrate;

forming a field plate above the first dielectric layer; and

self-aligning a gate electrode to the field plate,

wherein:

forming the first dielectric layer comprises:

forming the first dielectric layer to comprise:

a silicon-nitride layer; and

an aluminum-nitride layer.

Claim 20. (Currently Amended) The method of ~~claim 10~~ claim 11 wherein:

forming the gate electrode further comprises:

forming the gate electrode to be separated from the field plate by a distance of between approximately 20 and 400 nanometers.

Claim 21. (Currently Amended) The method of ~~claim 10~~ claim 11 wherein:

self-aligning the gate electrode comprises:

shortening a length of the field plate to between approximately 300 and 2000 nanometers.

Claim 22. (Currently Amended) The method of ~~claim 10~~ claim 11 wherein:

forming the field plate comprises:

forming the field plate to comprise titanium tungsten nitride.

Claim 23. (Original) A method of manufacturing a semiconductor component, the method comprising:

providing a semiconductor substrate;

forming a first dielectric layer above the semiconductor substrate;

forming a field plate comprising titanium tungsten nitride above the first dielectric layer;

simultaneously forming a first ohmic contact region and a second ohmic contact region above the semiconductor substrate;

forming a second dielectric layer above the field plate, the first dielectric layer, the first ohmic contact region, and the second ohmic contact region;

forming a hole in the second dielectric layer and between the first ohmic contact region and the second ohmic contact region to expose a portion of the field plate;

removing the portion of the field plate;

removing a portion of the first dielectric layer;

depositing a third dielectric layer over the second dielectric layer and in the hole;

etching the third dielectric layer to form a spacer inside the hole; and

forming a T-gate electrode in and over the hole;

wherein:

the spacer isolates the field plate from the T-gate electrode.

Claim 24. (Original) The method of claim 23 further comprising:

providing a semiconductor layer above the semiconductor substrate and below the first dielectric layer; and

forming a gate recess in the semiconductor layer,

wherein:

forming the T-gate electrode comprises:

forming the T-gate electrode in the hole and in the gate recess.

Claim 25. (Original) The method of claim 23 wherein:

forming the T-gate electrode further comprises:

forming the T-gate electrode to be separated from the field plate by a distance of between approximately 20 and 400 nanometers.

Claim 26. (Original) The method of claim 23 wherein:

forming the field plate comprises:

forming the field plate to have a length of between approximately 300 and 2000 nanometers.

Claim 27. (Original) The method of claim 23 wherein:

forming the second dielectric layer, forming the hole, removing the portion of the field plate, removing the portion of the first dielectric layer, depositing the third dielectric layer, etching the third dielectric layer, and forming the T-gate electrode comprise self-aligning the T-gate electrode to the field plate.